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Optoelectronic Technology Consortium

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[PRECOMPETITIVE CONSORTIUM FOR OPTOELECTRONIC INTERCONNECT TECHNOLOGY]

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1.0. Introduction

The Optoelectronic Technology Consortium has been established to position U.S. industry as the world leader in optical interconnect technology by developing, fabricating, integrating and demonstrating the producibility of optoelectronic components for high-density/high-data-rate processors and accelerating the insertion of this technology into military and commercial applications. This objective will be accomplished by a program focused in three areas:

1. Demonstrated performance

   OETC will demonstrate an aggregate data transfer rate of 16 Gbit/s between single transmitter and receiver packages, as well as the expandability of this technology by combining four links in parallel to achieve a 64 Gbit/s link.

2. Accelerated development

   By collaborating during the precompetitive technology development stage, OETC will advance the development of optical components, produce links for a multiboard processor testbed demonstration, and make samples available to User's Advisory Group members during 1994.

3. Producibility

   OETC's technology will achieve this performance by using components that are affordable, initially at <$100 per line, and reliable, with a line BER<10^{-15} and MTTF>10^6 hours.

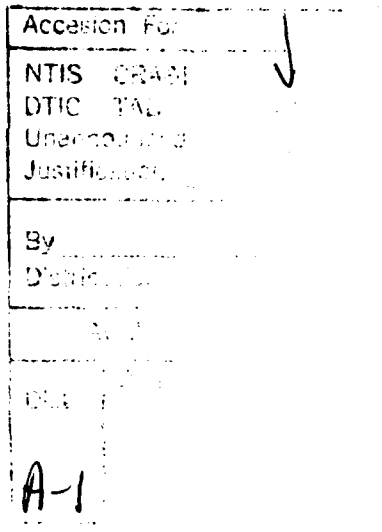
Under the OETC program, Honeywell will develop packaged AlGaAs arrays of waveguide modulators and polymer-based, high density, parallel optical backplane technology compatible with low-cost manufacturability.

The packaged AlGaAs modulator arrays will consist of a single fiber input, a 1 × 4 fanout circuit, four waveguide modulators, and four fiber outputs, all mounted on a ceramic header. The primary benefits to this approach are enhanced system reliability, particularly at high temperatures, and a device design that is highly producible due to the inherent process tolerance. Combined with the demonstrated high density of these devices when fabricated in arrays, this allows the development of compact, inexpensive, and reliable transmitter components.

The objective of the polyimide backplane development effort is to demonstrate a practical high density (>20 lines or channels per mm) parallel optical backplane facilitating (bandwidth × length/power) interconnect figures of merit between one and two orders of magnitude greater than would be attainable with state-of-the-art electrical interconnects. The effort will address both development of an ultimately manufacturable and environmentally tolerant optical backplane, and the optical interface concepts required for practical board-to-backplane optical

connection. The key functionalities, and compatibility with standard multiboard assembly practices will be demonstrated in a laboratory evaluation system.

Technical progress achieved during the current reporting period, and plans for the next reporting period, are summarized in the following sections.



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2.0. Progress Summary

2.1. AlGaAs Modulator Array Development
Task Leader: Dr. Charles Sullivan

During the current quarter, activities under this task have included design, material growth, device processing, and testing. The most important accomplishments and issues are identified below.

We have designed, laid out, and purchased a five-level mask set (named OETC-1, shown in Figure 1) based on a two-level metallization scheme using polyimide planarization (fabrication process designated PIC-1). This mask set contains a variety of designs for 1xn splitters and Mach-Zehnder interferometers, as well as standard Schottky contact and channel waveguide test structures. The principal objective of this mask set is to identify very early in our program all key issues and the magnitude of any problems which must be resolved to meet the program deliverable, performance, and producibility goals. We have received this mask set and verified that all device structures were delineated as designed.

The growth of epitaxial AlGaAs modulator structures will be carried out in our new low-pressure 3-inch OMVPE reactor purchased from Aixtron, which has just been brought on-line. The specifications for this reactor and the performance achieved during the acceptance tests are listed in Table 1. The uniformity, reproducibility and defect density parameters are particularly important in developing a producible device, and the reactor performance appears to be very promising in these respects. We have grown our baseline waveguide design (Figure 2) on five 3-inch GaAs wafers. Four out of the five grown wafers have very good surface morphology and will be used in the initial waveguide fabrication and test experiments using the OETC-1 mask set.

We have commenced our baseline modulator array process (PIC-1) using the OETC-1 mask set and OMVPE-grown wafers just described. Pilot epilayer samples have been characterized for waveguide attenuation by standard cutback techniques at 830 nm and show an acceptable planar waveguide loss of about 0.3 dB/cm. Measurements of singlemode waveguide attenuation are underway, but SEM analyses seem to suggest that further work is needed to reduce the roughness on the channel sidewalls to reduce the attenuation to the targeted 0.5 dB/cm range. The first-pass process run is expected to be compete by 12 October, and testing of the waveguide test structures and devices is expected to be completed by the end of October.

2.2. AlGaAs Modulator Array Packaging
Task Leader: Mr. John Lehman

Since the input to our AlGaAs modulator arrays must be polarized and single mode, this is the most challenging task of the packaging effort. Our baseline approach to the problem of feeding polarized light to AlGaAs modulator arrays is to use single mode, elliptical core, polarization-

maintaining fiber (Andrew Corporation D-Series) which is butt coupled to the AlGaAs waveguide. The elliptical core design was chosen because its mode field profile is very similar to that of the AlGaAs waveguide which minimizes coupling losses associated with mode field mismatch. Simulations will be performed to analyze the field coupling for different AlGaAs waveguide dimensions and for transverse, lateral, and longitudinal displacements. The simulations of the field coupling will result in estimates of the tolerances to maintain acceptable coupling and will be used as a goal in the design of the assembly technique. Fresnel losses and Fabry-Perot effects will be minimized in our packaged arrays by using index matching materials. A self-soldering technique will be used for active alignment of the fiber to the waveguide. This technique involves the incorporation of a resistive heater into the ceramic substrate, followed by the deposition and patterning of a soldering material. The fiber will be aligned, the solder heated to the melting point and then allowed to cool, soldering the fiber in place.

To date our OETC packaging effort has concentrated on verifying experimentally that high coupling efficiency can be achieved between the transmitter fiber and Honeywell's AlGaAs waveguides and refining the design for the self-soldering assembly technique which fixes the aligned fiber to the AlGaAs waveguide. Initial results indicate that high coupling efficiency can be achieved with our present selection of fiber and waveguide dimensions but that refinements of the packaging technique are needed to optimize and maintain high coupling efficiency.

We are reviewing our self-soldering assembly technique to make the refinements necessary to meet the submicron tolerances required as originally planned. The ceramic substrate, AlGaAs modulator array pedestal, and fiber holder are being designed and a meeting will be held in early October with Honeywell Military Avionics Division, the manufacturer of the ceramic substrates used in the packaging process, to review the designs.

2.3. Polymer Backplane Development
Task Leader: Dr. Julian Bristow

This task will use passive polymeric waveguides to implement high density routing components and interconnect structures. The task encompasses the demonstration of both the passive waveguide structures themselves, using commonly encountered backplane materials, and the interfacing of optical backplanes to waveguides located on daughterboards.

During this reporting period, we have identified the target waveguide dimensions for our backplane design. We aim to demonstrate the waveguides with heights of at least 20 microns, and comparable widths. The resulting waveguide densities, 20 to 50 channels/mm, approach an order of magnitude higher density than can practically be attained using standard optical fiber, yet are compatible with standard engineering tolerances. We have initiated experiments aimed at the demonstration of waveguides with the above stated dimensions. Our baseline waveguide material is polyimide, since this material is well established in the electronics industry, and has properties compatible with operation in military environments over tens of years without exhibiting degradation. We have selected preimidized polyimide materials, and have focused our initial experiments on deposition of single layers by spincasting, and drying out of the solvents. We have to date deposited films up to 10 μm in thickness. The optical characteristics of the

waveguides will be compared against those obtained from optimized multilayer deposition techniques in order to identify the optimum technique for depositing the optical waveguide layers on a range of commonly encountered backplane material systems, such as copper/polyimide. The waveguides are currently being fabricated on oxidized silicon wafers.

The baseline approach which has been identified for interfacing the optical backplane waveguides to waveguides on the daughterboards is to use expanded beam connectors with multiple channels sharing a given connector. Each channel is associated with a particular angle of propagation of the expanded beam with respect to the optical axis. Appropriate choice of optical components will allow negligible crosstalk, while allowing fractions of a millimeter positional misalignment. Despite the relaxed tolerances at the board-to-backplane interface, each channel must be located accurately with respect to the gradient index lens based connector. To ensure a manufacturable solution, the tolerances on misalignment should be as loose as possible. Since the interface between the waveguide and lens is at, or close to, the focal plane of the lens, this in turn requires that the dimensions of the guide be as large as possible. Thus a system level tradeoff must be performed in which increased board-to-backplane interconnection density can be effected at the cost of decreased tolerance to misplacement. We believe that compatibility with existing techniques for integrating boards with board level components requires dimensions at least 20 μm.

3.0. Second Quarter Plans

3.1. AlGaAs Modulator Array Development

Assuming good singlemode attenuation results with our present OMVPE materials, we will begin the growth of a variety of *pin* waveguide structures with the purpose of substantially improving the electrooptic conversion efficiency of our waveguide modulators without significantly degrading the optical throughput loss. Our long-term goal is to increase the (phase) modulation figure-of-merit from 2 – 4 deg/V-mm to >30 deg/V-mm which will allow us to reduce the active device length from about 15 mm to < 2 mm. We also plan to grow more wafers with the current structure for on-going device development activities and will concentrate on optimizing the device processing and growth procedures if the singlemode attenuation results do not meet our expectations.

The present OETC-1 mask set will be used in the next few months for process development and optimization activities, including initial experiments with *pin* waveguide structures.

A new mask set (to be named OETC-2) will be designed and laid out in the November-December timeframe to meet the form, fit, and function goals of the OETC. The specific device designs will be based on the test results for OETC-1/PIC-1 and beam-propagation method (BPM) simulation results. First-pass fabrication activities with this mask set are expected to commence in a few months and initial device test results will be available by the beginning of the third reporting quarter.

3.2. AlGaAs Modulator Array Packaging

We will finalize the design of our baseline packaging approach and will begin fabrication of the micro-fixtures used for the alignment of the D-shaped polarization maintaining fiber to the AlGaAs waveguides. Also, we will conclude our simulations of D-shaped fiber to GaAs waveguide field coupling efficiency, and will use the simulation results as a guide in specifying the alignment tolerances which must be achieved.

3.3. Polymer Backplane Development

During the next reporting period, we will be identifying polyimide materials systems which can be used to fabricate buried guides with low loss, and which will provide resistance of the waveguide to the effects of environmental factors such as humidity, large temperature swings and corrosive atmospheres. We will continue to fabricate polymer waveguides, with the goal of achieving a 20 μm thick guide with propagation loss <0.3 dB/cm. Although depositions to date have been on oxidized silicon substrates, we will begin optimization of waveguide fabrication processes on practical backplane material systems. This will involve incorporation of planarizing and buffer layer polymers into the basic waveguide fabrication process. We will initiate a design

of the routing components to be fabricated. As part of this design we will be looking at a tradeoff of the size or radius of curvature of routing elements versus the loss and plan to design, layout and purchase a mask set during the next quarter. We will also initiate the design of the board-backplane connector fixture.

4.0. Summary

During the current quarter, a first pass mask set has been generated for the fabrication of AlGaAs modulator arrays, and a process run has been initiated with this mask. The planar waveguide propagation loss in our OMVPE grown material has been shown to be acceptable, i.e. 0.3 dB/cm. Initial experiments in aligning polarization maintaining fiber to waveguide structures indicate that high coupling efficiencies should be attainable for our present selection of fiber and waveguide dimensions. Polyimide waveguide films have been deposited on oxidized silicon substrates with thicknesses up to 10 μm.

In the next quarter, we will complete and evaluate the first pass modulator array process run, and will design and layout a second mask to meet the form, fit and function goals of the OETC program. We will also begin the deposition of p-i-n waveguide structures with the intent of improving the electro-optic conversion efficiency of our waveguide modulators. In the area of packaging we will finalize our baseline approach, and will begin fabrication of the micro-fixtures used for fiber alignment. We will be fabricating 20 μm thick polymer waveguides, identifying materials for the deposition of buried guides, and will initiate the design of waveguide routing components and the board-backplane connection.

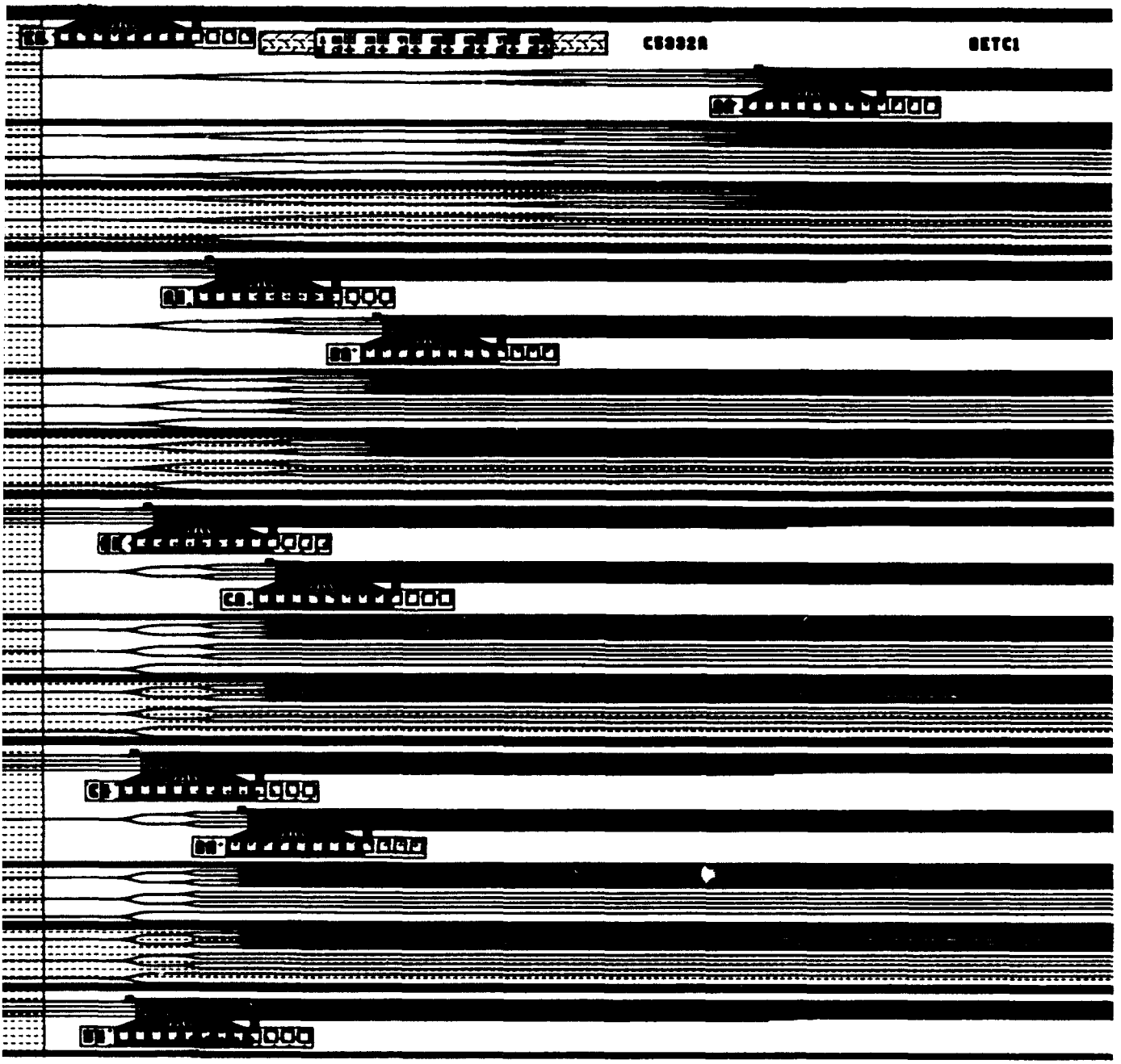

Figure 1.

Table 1. AIX 200 AlGaAs/GaAs Material Specifications and Performance

Parameter	Specification	Measurement	Comments
GaAs purity background cc 77K mobility	 $\leq 5 \times 10^{14}/cm^3$ $\geq 60{,}000\ cm^2/v\text{-}sec$	 $5 \times 10^{13}/cm^3$ $80{,}500\ cm^2/v\text{-}sec$	} Run 14
Uniformity: 3" thickness (Bragg mirror) composition ($Al_{0.3}Ga_{0.7}As$) doping GaAs:Si (n) GaAs:Zn (p)	 $\leq \pm 3\%$ $\leq \pm 1\%$ $\leq \pm 5\%$ $\leq \pm 5\%$	 $\pm 1.5\%$ $\pm 0.5\%$ $\pm 3.6\%$ $\pm 5\%$	Run 7 Run 5 Run 25 Run 24 } Specification and measurements exclude the outer 1/4" of 3" wafer
Reproducibility thickness (Bragg mirror) composition ($Al_{0.3}Ga_{0.7}As$)	 $\leq \pm 2\%$ $\leq \pm 1\%$	 $\pm 2\%$ $\leq \pm 0.3\%$	 Runs 6 & 9 Runs 5 & 7; difference is less than measurement resolution
Surface morphology (1 μm $Al_{0.3}Ga_{0.7}As$)	$<100\ defects/cm^2$	$<100\ defects/cm^2$	Run 5; appears to be significantly lower; not quantified yet
Photoluminescence intensity	Better than or equal to standard	20% better than standard	Run 20; AlGaAs waveguide structure used for comparison
Dopant range GaAs:Si (n) GaAs:Zn (p)	 5×10^{16} to $2 \times 10^{18}/cm^3$ 2×10^{16} to $5 \times 10^{18}/cm^3$	 3×10^{16} to $2.4 \times 10^{18}/cm^3$ 2×10^{16} to $8 \times 10^{18}/cm^3$	 Runs 27 & 31 Runs 23 & 24
Interface abruptness x-ray: 34Å/34Å SL PL: 30, 50, 80, 120Å QW	5.6Å (2 monolayers)	x-ray: ≤10Å PL: 3 – 4 monolayers	Run 28 Run 34 } Still working with AIXTRON to demonstrate this parameter

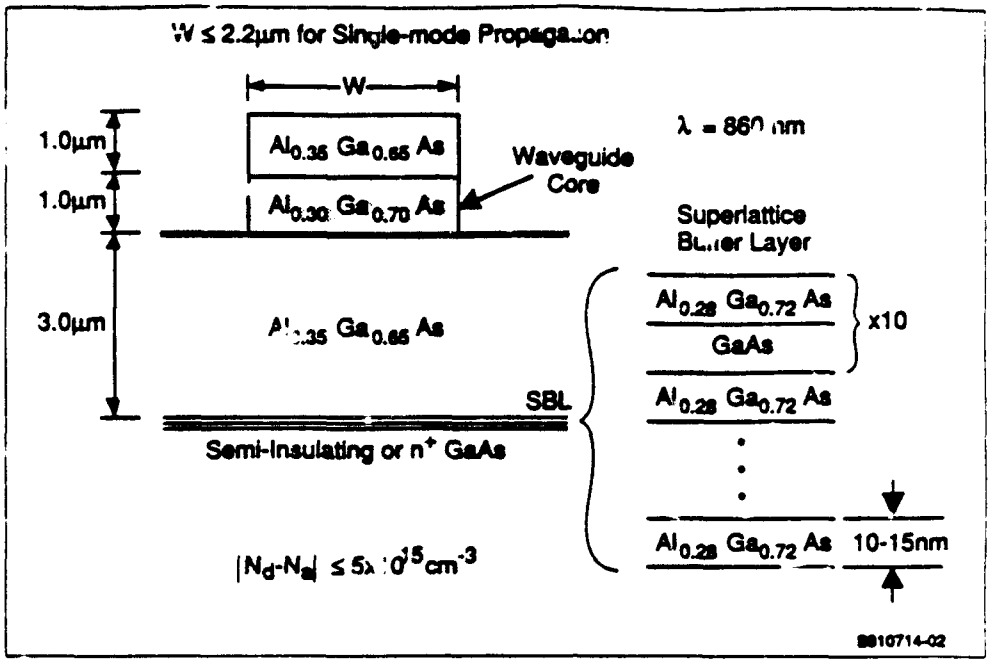
W ≤ 2.2μm for Single-mode Propagation
W
1.0μm
1.0μm
3.0μm
Al0.35 Ga0.65 As
Al0.30 Ga0.70 As
Waveguide Core
λ = 860 nm
Superlattice Buffer Layer
Al0.35 Ga0.65 As
SBL
Semi-Insulating or n+ GaAs
|Nd-Na| ≤ 5x10^15cm^-3
Al0.28 Ga0.72 As
GaAs
x10
Al0.28 Ga0.72 As
Al0.28 Ga0.72 As
10-15nm
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Figure 2.